ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit device including a plurality of memory cells, each having a storage MOSFET holding information in a gate of the storage MOSFET, a write transistor supplying a write information voltage corresponding to the information to the gate storage MOSFET, and a capacitor having first and second terminals. Word lines and data lines are coupled with the memory cells. The first capacitor terminal is coupled with one of the word lines and the second capacitor terminal is coupled with the gate of the storage MOSFET. In a read operation of the semiconductor integrated circuit device, the gate voltage of the storage MOSFET is boosted by a transition of the word line from a first voltage to a second voltage greater than the first voltage.